Temperature-Dependent Modeling of Gallium Arsenide MESFET's

Steven M. Lardizabal, *Member, IEEE*, Allen S. Fernandez, and Lawrence P. Dunleavy, *Member, IEEE*

Abstract— **A complete temperature-dependent small signal model extraction methodology is used to achieve accurate circuit level simulations of metal semiconductor field-effect transistor (MESFET) amplifier performance over temperature. The procedure applies a previously described field-effect transistor (FET) modeling approach to predict the performance of a small signal amplifier over a −55°C to 100°C temperature range. This work includes a description of the MESFET equivalent circuit element thermal coefficients along with an amplifier simulation. Therefore, for the first time, a clear correspondence between circuit level simulation and measured results over temperature are published together. A new comparison of published temperature-dependent data shows a common agreement for amplifier gain variations of 0.015 dB/°C/Stage for a broad range of designs from 400 K down to cryogenic levels (77 K).**

I. Introduction

THE gallium-arsenide (GaAs) metal-semiconductor field-effect transistor (MESFET) is currently the most common active device in monolithic microwave/millimeter-wave integrated circuits (MMIC's). Accurate field-effect transistor (FET) models are needed to reduce design (CAD) and development costs of MMIC, as well as hybrid microwave integrated circuit (MIC), applications that require performance over a wide temperature range. For example, a typical military temperature range is from −55°C (218 K) to 125°C (398 K). Some commercial applications may require similar or even more stringent temperature extremes. There is also continuing interest in cryogenic temperature operation, since device performance improves at very low temperatures. In contrast, traditional MMIC designs consider only room temperature operation, due to the general unavailability of temperature-dependent FET CAD models. This practice necessitates expensive post fabrication temperature characterization of MMIC's, and may require a temperature compensation network at the subsystem level. While some work toward developing temperature-dependent FET models has been reported [1], [10], more work is needed to develop a more complete understanding of FET temperature behavior and to better establish practical temperature-dependent FET modeling and circuit design approaches. This paper addresses this need.

One approach is to use an empirical model for temperature-dependent simulations of the GaAs MESFET [2], but these curve fit models require experimental data that the designer may not have. To be sure, commercially available software exists that uses a default set of thermal coefficients to describe performance variations due to ambient temperature changes, but what amount of variation in performance is expected over temperature, and for what bias and temperature conditions are the default model coefficients defined for? To consider such trends, physics-based theoretical simulations for device performance over temperature have been advanced to a high level of accuracy and efficiency, but these physics-based models are not widely available for design analysis. As a consequence, temperature-dependent simulation of circuit-level performance for MMIC's and MIC's is not a routine procedure in design even though some capability exists to do so.

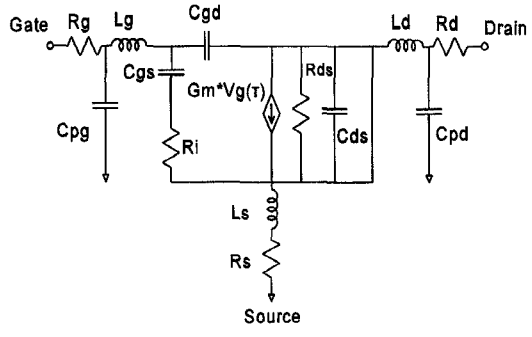

Fig. 1. Small-signal equivalent circuit model of the FET.

This paper examines small signal temperature-dependent MESFET models from an experimental point of view. The basic model used is shown Fig. 1. Other topologies may include additional parasitic elements; however, this model includes all of the dominant parameters and is shown to be quite adequate for the MMIC devices considered herein. Another advantage of this topology is that it enables a direct extraction of equivalent circuit parameters from measured data without requiring optimization.

The presented procedure is an application of the approach described elsewhere [1] and [2], but now applied to the circuit-level simulation problem. In this paper we use the equivalent circuit parameter (ECP) extraction approach and determine thermal coefficients for the ECP's. A review of previously reported work is given in Section II to identify and compare several aspects of the temperature-dependent modeling of the GaAs MESFET. Examples from previously reported temperature induced gain variations for a broad range of circuit designs are compared with measured results given in this work. From this comparison, a simple empirical relation

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TABLE I
COMPARISON OF PREVIOUS TEMPERATURE DEPENDENT GaAs MESFET INVESTIGATIONS

Author(s)	Temperature Range (°C or K)	Model: Theory or Experiment	Intrinsic Equivalent Circuit Parameters (Sign of Thermal Coefficient +/-)					
Theory			Cgs	gm	Rds	Cdg	Cds	tau
Hirose [22]	300 to 500K	Theory	+	-	*	*	*	*
Curtice [3]	320 to 420K	Theory	-	-	*	*	*	*
Atherton, Snowden [4]	8 to 127K	Theory	+	-	+	+	*	*
Cryogenic Research								
Liechti and Larrick [6]	90 to 300K	Experiment	-	-	+	+	*	*
Wienreb [7]	20 to 300K	Experiment	+	-	+	*	*	*
Lasker et. al. [8]	70 to 300K	Experiment	+	-	+	-	*	*
MIL-SPEC								
Pengelley [10]	-55 to 125	Experiment	+	-	*	*	*	*
Anholt and Swirhun [1]	-70 to 110	Experiment	+	-	+	+	+	+
Fernandez and Dunleavy [21]	-55 to 125	Experiment	+	-	+	+	+	+

*Element variation not reported.

for the expected gain variation of a GaAs MESFET amplifier is tested. Next, in Section III, a temperature-dependent measurement based model development is described for two different MESFET devices. These included a 0.25×400 μm ion-implanted power FET made up of 12 gate fingers. For this device the equivalent uniform doping density and Hall mobility were 5×10^{17} cm^{-3} and 3250 cm^2/V-sec, respectively. The other device, a low noise MESFET, had gate dimensions of 0.5×300 μms, with four gate fingers. The equivalent uniform doping density and Hall mobility of this second device were 2.75×10^{17} cm^{-3} of 3800 cm^2/V-sec, respectively. Both devices are on 100 μms thick GaAs substrates, and each uses two via hole source grounds per FET. ECP's for these devices are extracted over a -55 to 125°C temperature range from 40 GHz S-parameter data. Finally, in Section IV results are compared to measurements over temperature for MMIC amplifier simulations based on one of the developed FET models.

II. PREVIOUS RESEARCH

Research into the temperature-dependent performance and characteristics of GaAs MESFET's has been approached theoretically through the development of two-dimensional (2-D) Poisson's equation solving simulators and by experiments that relate device measurements to an equivalent circuit parameter model. Both solutions are valuable to the investigation of device performance with respect to temperature. In this section, the results of both numerical device simulations and experimental observations are reviewed. The selected results span a range of temperatures from 500 K down to cryogenic levels (4 K).

Table I lists several of the previous works on temperature-dependent modeling of GaAs MESFET's. The works of Curtice [3] and also Atherton *et al.* [4] simulate the governing equations of semiconductor physics and heat transfer. Results from [4] are particularly notable for an agreement with temperature-dependent measurements. That work simulates device self-heating effects and ambient temperature effects on device performance. S-parameters for these numerical models are derived from the admittance matrix that is determined by the Fourier decomposition method [5]. This allows extraction of an equivalent circuit model from the simulated admittance matrix or the equivalent simulated S-parameters. In general, however, device models are more quickly developed experimentally.

An experimentally based extraction of an equivalent circuit parameter model for a GaAs MESFET efficiently provides an accurate means of thermal simulation. The extraction method is advantageous, because of the speed of processing versus the numerical solution. Also, when the parameters are extracted versus temperature a single vector of linear thermal coefficients for the circuit parameters is often sufficient to describe the FET's performance over temperature. The earliest experimental characterizations were performed at cryogenic temperatures [6]–[9]. The work of Pengelly [10] shows the first practical CAD-related implementation of temperature-dependent MESFET modeling in the -55 to 125°C range. Recent works, [1] and [2], have begun to publish tables of equivalent circuit

parameters and their related thermal coefficients for modeling purposes.

A review of the papers in Table I show classifications that may be more or less important depending upon the application. These applications range from circuit design and validation issues to FET modeling and fabrication issues at specific ambient temperature-dependent simulation ranges. Several issues to answer when using a temperature-dependent FET model include: How are equivalent circuit parameter values determined? At what ambient temperatures was device performance investigated? Do the models show agreement with physical factors such as electron saturation velocity, low-field mobility, electron trapping effects (threshold voltage shifts), changes in Schottky barrier height, and unity current gain cut-off frequency? Are the resulting FET models used for circuit modeling, and how well do the simulations predict circuit temperature performance? Are bias dependencies included, and what is gained by performing such an analysis?

Differences with respect to the above issues generally appear as follows: often a complete set of equivalent circuit elements and their thermal coefficients are not given; there is a minor discrepancy in the determination of either the linearity or nonlinearity of these thermal coefficients; whether or not gate-to-source capacitance has a positive or negative thermal coefficient above $T = 300$ K and at cryogenic temperatures; and the use and validation of the temperature-dependent device model in a circuit simulation.

From the list of reported temperature dependencies shown in Table I, it is noted that the dominant changes are the same in every investigation. It has been clear for some time that an increase in the ambient temperature results in a reduction of the saturated carrier velocity, and a drop in the transconductance, G_m. It is also clear that the output resistance $R_{\rm ds}$ increases with the ambient temperature. In the case of the gate-to-source capacitance $C_{\rm gs}$ an increase may be expected due to a decrease in the depletion depth as the Schottky barrier height decreases with increasing temperature. However, $C_{\rm gs}$ is bias dependent and the quiescent operating point may be at a point where $C_{\rm gs}$ exhibits a negative thermal coefficient for increasing temperature. The variation of $C_{\rm gs}$ may also be slight, as with $C_{\rm dg}$ and $C_{\rm ds}$. The small variation of $C_{\rm gs}$ is also reflected in the relative insensitivity of S_{11} to temperature change.

In addition to the sign of the gradient given in Table I, the curvature of the thermal variation also introduces differences when comparing results. The temperature dependence of the ECP's is found to be only mildly nonlinear, except where trapping states affect device performance. The temperature variation of the ECP's has been fit by both linear and nonlinear equations. From Table I, [1] and [2] have shown a linear temperature dependence to be useful. Also from Table I, [8] includes cryogenic performance expressed in a nonlinear form as $P(T/T_0)^{\alpha}$. Relating the linear B coefficients of [1] to the α coefficients of [8] through a Taylor series expansion of P shows [1] and [8] to be complimentary, especially for $-0.13 < \alpha < -0.17$ range reported in [8]. In the case where trapping effects significantly alter device characteristics it may be decided to fit two sets of data by linear thermal coefficients in a piecewise manner. The increased number of data points required to determine where trapping states effect device characteristics is not necessary for most designs since performance at the temperature extremes is usually most important. With carefully planned measurements the resulting window of uncertainty is unlikely to detrimentally affect the end performance of the intended circuit utilizing these components.

Although no circuit level simulation of temperature performance is given in [1], that work presents the most comparisons of experimental results on physical factors, such as: electron saturation velocity, low-field mobility, electron trapping effects (threshold voltage shifts), changes in Schottky barrier height, and unity current gain cut-off frequency. Results from Laskar *et al.* [8] for the electron saturation velocity extend the information given by Anholt [1] down to cryogenic temperatures.

Of the nine investigations listed in Table I, five include a demonstration of circuit simulation and measurements over temperature. Specifically, Liechti [6], Wienreb [7], and Angelov [9] report not only on model performance, but also on circuit design and measurement techniques for cryogenic amplifiers. This paper and [10] also show comparisons of amplifier measurements and simulations over the -55 to 100°C temperature range. The quality of the comparison depends upon the agreement of the initial room temperature simulation to the fabricated amplifier's performance. While the temperature dependencies of amplifier gain may be simulated, the actual data usually reflects differences, probably due to process variation and/or passive element model deficiencies. A clear correspondence between circuit level simulation results and measured data is completely defined here.

Gain variation is the most common temperature-dependent factor affecting circuit design. For staged amplifier configurations, temperature effects are critical, because the gain variation is multiplicative as in (1), [11]

$$\Delta G_T = \gamma \cdot \Delta T n \tag{1}$$

where γ is the loss per degree Celsius per stage, $\Delta T = (T - T_0)$, T is the ambient temperature, T_0 is 290 K, and n is the number of amplifier stages. Therefore, it is useful to have a reliable empirical relation to estimate design performance even before circuit level simulation. Since the thermally induced variation of the FET is usually the dominant element of circuit temperature dependence, a comparison of the gain variation may be useful to designers. Table II lists values of gain variation coefficient observed for GaAs MESFET amplifiers from several works. The first six references of Table II indicate a consistent trend for GaAs MESFET amplifier performance. The work of Cappello and Pierro [13] shows about half the variation in gain. Next, the series feedback amplifier data of Angelov *et al.* [9] is less temperature variable by a factor of three. Those series feedback amplifiers were intended for low-noise cryogenic application and were designed with suspended microstriplines. Finally, the work of Honjo [14] shows a full order of magnitude decrease in the gain variation achieved between elevated and reduced temperatures by designing temperature compensation into a resistively loaded amplifier.

TABLE II
GAIN VARIATION COEFFICIENT FOR VARIOUS REPORTED GaAs MESFET AMPLIFIERS

Reference Data	Amplifier Type	Gain variation coefficient (dB/°C/Stage)
Liechti and Larrick[6]	3 Stage, reactive	0.018
Wienreb[7]	2 Stage, reactive	0.014
Alpha Semiconductor[11]	general guideline	0.015
Pengelly[10]	2 Stage, parallel feedback	0.014
	Travelling Wave Amplifier	0.016
Crescenzi et. al.[12]	Balanced, T<25°C	0.012
	Balanced, T>25°C	0.016
Lardizabal et. al. (this work)	1 Stage, reactive	0.016
Capello and Pierro[13]	1 Stage, reactive	0.0069
	5 Stages, cascaded	0.0073
Angelov et. al.[9]	2 Stage, series feedback	0.005
Honjo[14]	2 Stage, resistively loaded	0.0012

III. MEASUREMENT-BASED MODEL DEVELOPMENT

The development of a temperature-dependent equivalent circuit parameter model of the GaAs MESFET is pursued here for small-signal amplifier simulations. DC current versus voltage (I–V) data measured over temperature allows an initial characterization of thermally induced performance changes. The temperature-dependent effect on dc I–V data by the gate threshold voltage and the electron saturation velocity has been demonstrated [15]. Trapping effects at low temperatures have also been observed in threshold voltage data on HEMT's [1]. Measured dc I–V curves versus temperature showed no sign of nonlinear threshold voltage shifts, associated with deep level trapping, for the devices studied here.

The RF measurement setup used includes a Cascade Microtech probe station with a pair of coplanar (ground–signal–ground) RF probes, a Hewlett-Packard 8510B Network Analyzer, a dual power supply, and a Hewlett Packard data acquisition facility. A Temptronix TPO 315A thermal chuck and temperature controller is used for cycling from 25°C to 125°C. A line-reflect-match (LRM) calibration procedure is performed at each temperature to minimize uncertainties related to calibration drift [16] and with respect to the match standard [17]. As previously indicated, there are two devices that are measured in this study: a 0.25 μm × 400 μm power MESFET (characterized from 45 MHz to 40 GHz) and a 0.5 μm × 300 μm low-noise MESFET (characterized from 45 MHz to 26.5 GHz). Operating quiescent bias conditions of 50% $I_{\rm dss}$ and 15% $I_{\rm dss}$ were applied, respectively, to the power MESFET and the low-noise MESFET.

In the past, most equivalent circuit models were extracted via optimization routines provided by CAD software packages such as LIBRA$^{\rm TM}$ or SUPER-COMPACT$^{\rm TM}$. It has been shown that equivalent circuit parameters extracted in this manner can depend on the starting values assigned [18]. This form of modeling introduces an unwanted level of uncertainty with respect to the uniqueness and physical meaning of the equivalent circuit parameters.

Alternatively, by using the model topology of Fig. 1, it is possible extract each equivalent circuit parameter of the FET model directly from measured data [19]–[21]. Such a model extraction procedure is adopted here to extract a robust set of temperature-dependent equivalent circuit parameters. The procedure used here for model parameter extraction is as follows.

1) Determine extrinsic elements R_g, L_g, R_s, L_s, R_d, L_d based on "cold FET" biased S-parameter measurements ($V_{\rm ds} = 0.0$, $V_{\rm gs} > 0.0$).
2) Use matrix algebra to determine intrinsic y-parameters from measured S-parameters and extrinsic elements determined in step 1).
3) Calculate intrinsic element values ($R_i, C_{\rm gs}, C_{\rm ds}, C_{\rm dg}, g_m, R_{\rm ds}$) from intrinsic y-parameters. Calculation is possible at each measurement frequency. Element values are selected as an average value over a specific frequency range.

The equivalent circuit parameters are extracted from measurements taken at several temperatures. When the temperature of the wafer chuck is adjusted the bias is removed as a practical matter, since bias is introduced through the RF probes. The RF probes are lifted as a precaution, because expansion of both the wafer and the thermal chuck may cause excess probe skating that can result in damage to the probes and/or the device under test. The probes are repositioned after the wafer has reached the desired temperature. The applied bias voltages at the gate and drain are held constant over temperature and the change in drain-to-source current, $I_{\rm ds}$, is recorded. Additionally, the network analyzer calibration is verified periodically using the thru-line standard to check for significant drift in the measurement system performance.

TABLE III
INTRINSIC EQUIVALENT CIRCUIT PARAMETER THERMAL COEFFICIENTS, B (10^{-3}/°C)

025×400μm Power MESFET[1]			025×300μm Low-Noise MESFET[2]		
Nominal Intrinsic Parameter Value		Thermal Coefficient, B	Nominal Intrinsic Parameter Value		Thermal Coefficient, B
G_m	(71.4 mS)	-1.73	G_m	(25 mS)	-1.58
C_{gs}	(369.1 fF)	0.02	C_{gs}	(209 fF)	0.63
C_{gd}	(28.1 fF)	0.42	C_{gd}	(44 fF)	0.21
C_{ds}	(102.0 fF)	0.20	C_{ds}	(194 fF)	0.34
R_{ds}	(167.6 Ohm)	1.62	R_{ds}	(360 Ohm)	1.63
R_i	(1.63 Ohm)	4.72	R_i	(5.45 Ohm)	1.77
τ	(2.12 psec.)	1.49	τ	(1.93 psec.)	1.98
f_t	(28.25 Ghz)	-1.8	f_t	(33.53 Ghz)	-2.8

[1] V_g = -0.87 V, V_{ds} = 5 V.
[2] V_g = -1.1 V, V_{ds} = 3 V, T > 25°C.

Table III lists the thermal coefficients associated with the extracted parameter variations for both devices studied here. The parameters are fit well by a linear temperature dependence. The resulting temperature-dependent equations for each ECP were inserted into a commercially available computer-aided-design software model, to predict MESFET small signal performance versus temperature.

The temperature-dependent performance of the simulated MESFET is demonstrated here over the −55 to 100°C temperature range. The dominant temperature effects are the decrease in the magnitude of S_{21} and S_{22}. Figs. 2 and 3 show the agreement between the measured and modeled S_{22} and S_{21}, which are the parameters most affected by the ambient temperature change. The excellent tracking of the temperature-dependent response of the linear model is evident. Only a slight phase change is exhibited for S_{11} and S_{22}, due to variations in RF probe placement. While the phase of S_{21} differs from the measured device performance by 12° at 40 GHz, the tracking of the temperature change is good. This error is most likely due to the inaccuracy associated with the calculation of the delay time, τ. By consistently applying the extraction procedure at each temperature it is expected that while some uncertainty in the value of τ exists, the thermal induced variation is correct due to our methodology.

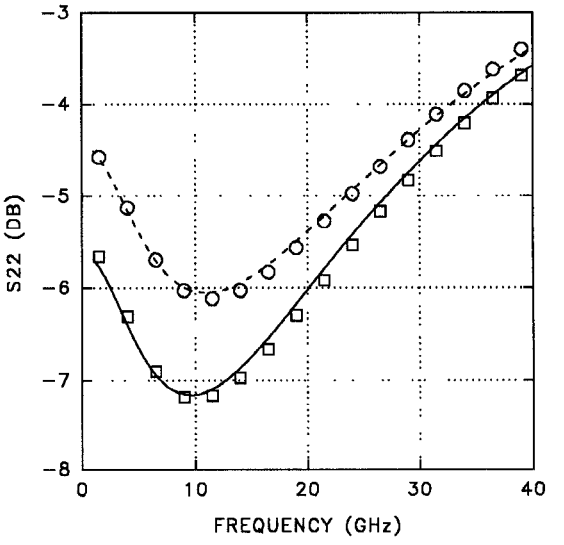

Fig. 2. Small-signal model performance over temperature S_{22} (data 100°C ○, and −55°C □) and S_{22} (100°C dashed line and −55°C solid line are simulations).

IV. AMPLIFIER RESULTS

The test vehicle for validating the temperature-dependent model is a single stage amplifier. The design layout is simple and therefore reduces the uncertainty in accounting for the temperature variations due to passive structures. The design is reactively matched for power gain at 34 GHz. The input and output networks use open microstrip stubs for tuning. DC bias is provided by shunt microstrip stubs. Two resistors at the gate bias line are used to stabilize the FET, and detune the dc bias line. MIM capacitors are used for dc blocking at input and output ports and RF shorts at the dc bias points. The nominal substrate height is 100 μms, and connections for RF testing are provided by ground-signal-ground RF wafer probes.

Ideally, the temperature-dependent modeling process of the preceding section assumes good correlation between the MESFET's used for the amplifier design and the devices resulting upon manufacture of the circuit. Additionally, the measured FET data must be accurately deembedded from the measurement system. The room temperature comparison of the measured amplifier data and the simulation is shown in Fig. 4. The resulting amplifier simulation is compared to measured amplifier data in Fig. 5 over the −55°C to 100°C temperature range. For this test case the measured amplifier gain variation is 0.0167 dB/°C/Stage. The simulated gain variation due to changes in the dielectric constant of the chip, the resistor

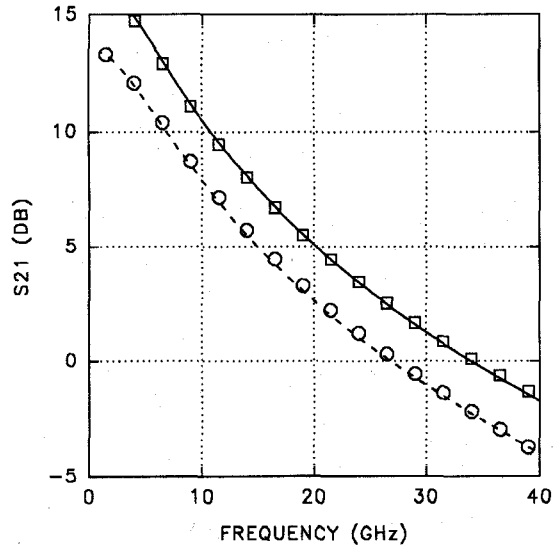

Fig. 3. Small signal model performance over temperature, S_{21} (dB) (○, □ data 100°C and −55°C) and S_{21} (dB) (100°C dashed and −55°C solid lines are simulations).

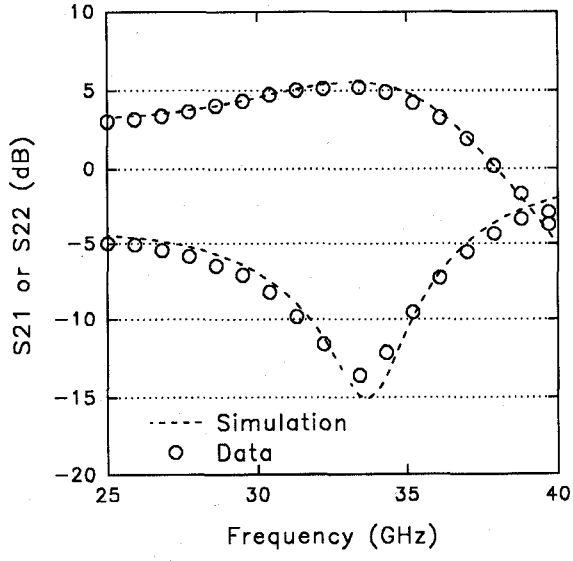

Fig. 4. Measured and modeled amplifier performance at room temperature, data is shown as open circles.

value, and the MIM capacitor values accounted together for 0.001 dB/°C/Stage variation in the small signal gain. Good agreements between the measured and the modeled small signal gain, DB[S_{21}] and the output match, DB[S_{22}] are shown.

V. Conclusion

In this paper we have provided a demonstration of a complete temperature-dependent small signal model extraction procedure for the MESFET. The accuracy and usefulness of the model are shown by example for a MESFET amplifier. From a survey of available data on MESFET amplifier performance we find that an empirical design equation for expected gain variation is surprisingly consistent for a broad range of packaged (MIC) and monolithic (MMIC) technology. Therefore a designer using a set of default thermal coefficients for a given device can determine if the simulation is reasonable. Differences from the most commonly observed gain variations

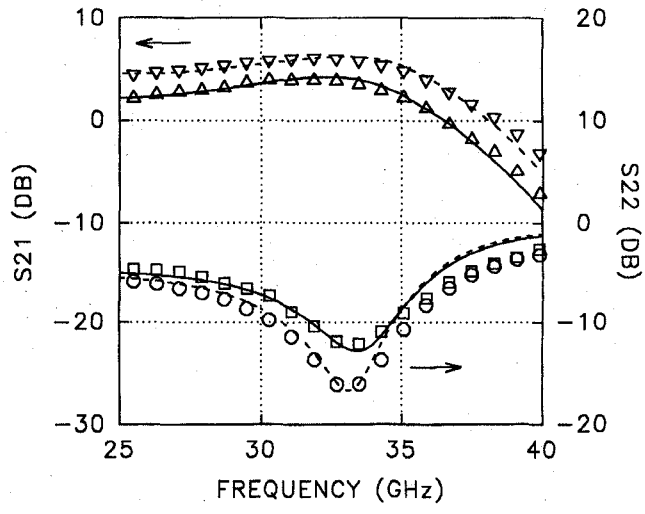

Fig. 5. Measured and modeled amplifier performance. Data is shown as □ S_{22} and △ S_{21} at $T = 100°C$, and ○ S_{22} and ▽ S_{21} at $T = -55°C$; simulations are indicated by dashed lines at $T = -55°C$, and solid lines at $T = 100°C$.

are identified due to feedback and more severely due to resistive loading at the output. With the recent publishing of a wide variety of temperature-dependent data, designers should not go without temperature modeling where performance over a range of temperatures is required.

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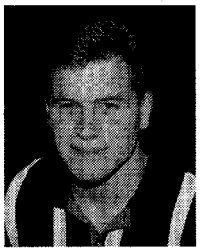

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